Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **BALANCE**
2. **INPUT –**
3. **INPUT +**
4. **V –**
5. **BALANCE**
6. **OUTPUT**
7. **V +**

**.073”**

**.042”**

**DIE ID**

**2 1 7**

**3 4 5 6**

**Top Material: Al**

**Backside Material: Au or Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: C**

**APPROVED BY: DK DIE SIZE .042 X .73” DATE: 11/9/21**

**MFG: NATIONAL THICKNESS .014” P/N: LF157**

**DG 10.1.2**

#### Rev B, 7/19/02